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Automotive Discrete Group (ADG)
Power Transistor Division

Process Change Notification

Technology transfer of RF DMOS LV 1931/1941 line from 6” CT6 fab to 6” SG6 (Singapore) FAB

Dear Customer,

Following the continuous improvement of our service and in order to increase productivity, we announce that *RF DMOS LV 1931/1941 line*, currently manufactured in Catania will be performed in ST’s Ang Mo Kio (Singapore) FAB.
Wafers produced in Ang Mo Kio (Singapore) FAB, guarantee the same quality and electrical characteristics as per current production.

In the next pages, we are reporting the qualification plan to reach full maturity.

The change has been classified as **Class 1** according to the ST internal rules.

	Assessment of impact on Supply Chain regarding following aspects - contractual agreements - technical interface of processability / manufacturability of customer - form, fit, function, quality performance, reliability	**Remaining risks on Supply Chain?**	
ID	**Type of change**	**No**	**Yes**
SEM-PW-13	Move of all or part of wafer fab to a different location/site/subcontractor	P	

P=PCN

The qualification report of the change will be available July 2020 according the attached qualification plan.

Sincerely Yours!

Tech name **Technology Transfer in ST's Ang Mo Kio (Singapore) FAB**	
ST Part number:	ST PNs: *DMOS LV 1931/1941 line* Package: **All the Packages**
Reason and background of the change	To increase flexibility and increase Capacity
Detailed description of change(s), including affected type of changes	The Diffusion Process and Wafer Testing for *DMOS LV 1931/1941 line* technology will be performed in ST's Ang Mo Kio (Singapore) FAB.
Impact on form, fit, function, or reliability.	No Impact - No Change
Datasheet	No Impact - No Change
Benefit of the change	Capacity and flexibility increase.
Qualification Plan and Implementation date for change	The qualification will be completed in agreement with JEDEC and internal spec 0061692 specification (See attached RELIABILITY PLAN)
Traceability Information	By QA Number
PPAP Update	NA

PACKAGE/PRODUCT RELIABILITY PLAN

Reliability evaluation for Transfer RF Power DMOS silicon lines 1931/1941 from CT6" to SG6" (Mix Flow)

Package used : M174 / M177 manufactured in ST BOUSKOURA plant (MOROCCO)

Site for Reliability assessment: CATANIA

Test vehicle details:
- **LOT1: silicon line 1931 - in M174 package**
- **LOT2: silicon line 1931 - in M177 package**
- **LOT3: silicon line 1941 - in M174 package**

TEST #	TEST Descripition	Reference	LOT1	LOT2	LOT3	Sample Size per lot	TEST Condition	Requirement	pass conditions	Description
1	Pre- and Post-Stress Electrical Test	User Specification	x	x	x	All qualification parts tested per the requirements of the appropriate device specification.			zero rejects	The test is performed as specified in the applicable stress reference at room temperature
2	External visual	JESD22 B-101	x	x	x	All devices submitted for testing			zero rejects	
3	High Temperature Reverse Bias **(HTRB)**	JESD22 A-108	x	x	x	45	Ta=175°C , Vbias=80% of max breakdown voltage	1000 hours	zero rejects	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations.
4	High Temperature Gate Bias **(HTGB)**	JESD22 A-108	x	x	x	45	Ta=175°C, Vgs= Vgsmax	1000 hours	zero rejects	
5	High Temperature Storage Life **(HTSL)**	JESD22 A-103	x	x	x	45	Ta=175°C	1000 hours	zero rejects	
6	Temperature Cycling **(TC)**	JESD22 A-103	x	x	x	25	Ta= –65°C / +150°C (1h cycle - 30min at extreme temp.)	500 cycles	zero rejects	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.
7	**ESD**	ESDA-JEDEC_ JES-001 ANSI-ESD S5.3.1	x			3	HBM CDM	-	-	
										Rel - 37/2018RW **Issued 25/Jan/2018**